Freie Universität Bozen
Libera Università di Bolzano
Università Liedia de Bulsan

COURSE DESCRIPTION – ACADEMIC YEAR 2024/2025

Course title	Computer Architecture
Course code	42418
Scientific sector	ING-INF/05
Degree	Bachelor in electronic and cyber-physical systems engineering
Semester	1st
Year	III
Academic year	2024/2025
Credits	6 CFU
Modular	No

Total lecturing hours	40
Total exercise hours	20
Attendance	
Prerequisites	Mathematical Analysis I, Linear Algebra, Physics I
Course page	https://www.unibz.it/en/faculties/engineering/bachelor-electronics-cyber-physical-systems-engineering/course-offering/

Lecturer	Dr. Nicola Gigante
Contact	Nicola.Gigante@unibz.it
Scientific sector of lecturer	INF/01
Teaching language	English
Office hours	tbd
Lecturing assistant (if any)	none
Contact LA	none
Office hours LA	none
List of topics	• Binary arithmetic (two's complement, IEEE 754 floating point format, issues with floating-point computations) • General computer architecture (Von Neumann architecture; CPUs; bus; memory; peripherals) • Instruction set architecture (CISC vs RISC architecture; instructions: data-movement, control-flow, arithmetic/logic; common ISAs: introduction to x86, ARM, RISC-V; assembly programming). • CPU architecture (control unit, registers, ALU; fetch-decode-execute cycle; pipelining; super-scalar architecture; branch prediction; out-of-order execution; caches). • Memory and buses (static vs dynamic memory; serial/parallel buses; synchronous/asynchronous buses; bus arbitration strategies; example of buses: PCI, PCI-Express, USB). • Other topics (multi-processor and multi-core architectures; introduction to GPUs).
Teaching format	Frontal lectures, exercises, and laboratories

Specific educational objectives	The course aims at providing students with the fundamental notions of the organization and architecture of modern computer systems. The students will first acquire basic knowledge about the design and implementation of sequential logical circuits, to then proceed to learn how modern CPUs are organized and

	structured. Students will learn how to interface to the CPU at the lowest level possible by means of Assembly programming. Modern and common architectures are introduced, such as x86, ARM, and RISC-V. An architectural understanding of how the CPU interacts with the main memory and peripherals through the system bus is provided.

Learning outcomes	**Knowledge and understanding** The student knows how sequential digital circuits are structured and designed. They know how modern CPU architectures are structured and organized and how to write Assembly programs for at least one common architecture. **Applying knowledge and understanding** The student is able to use the knowledge acquired to create sequential circuits, to write Assembly programs, and to understand how the tradeoffs in the CPU architecture design affect the performance of their programs. **Communication skills** The student is able to present the competencies acquired with vocabulary appropriate to the topic. **Learning skills** The student is able to use the tools and reasoning techniques acquired to extend his/her knowledge.

Assessment	Written exam.
Assessment language	English
Evaluation criteria and criteria for awarding marks	The valuation criteria will be: accuracy of the answers given to the written exam, with particular attention to the resolution procedure adopted.

Required readings	Materials provided by the teacher.
Supplementary readings	Supplementary readings will be provided by the lecturers prior to lectures.