Syllabus

Course description

Course title	Computer Architecture
Course code	42418
Course title additional	
Scientific sector	ING-INF/05
Teaching language(s)	Italian
Degree course	Bachelor in Electronic and Information Engineering
Other degree courses (loaned)	
Lecturer(s)	Dr. Nicola Gigante, Nicola.Gigante@unibz.it https://www.unibz.it/en/faculties/engineering/academic-staff/person/43773
Teaching assistant(s)	
Semester	1
Course year	3
CP	6
Teaching hours	40
Lab hours	20
Individual study	90
Planned office hours	18
Contents summary	• Binary arithmetic (two's complement, IEEE 754 floating point format, issues with floating-point computations) • General computer architecture (Von Neumann architecture; CPUs; bus; memory; peripherals) • Instruction set architecture (CISC vs RISC architecture; instructions: data-movement, controlflow, arithmetic/logic; common ISAs: introduction to x86, ARM, RISC-V; assembly programming). • CPU architecture (control unit, registers, ALU; fetch-decode-execute cycle; pipelining; superscalar architecture; branch prediction; out-of-order execution; caches). • Memory and buses (static vs dynamic memory; serial/parallel buses; synchronous/asynchronous buses; bus arbitration strategies; example of buses: PCI, PCIExpress, USB). • Other topics (multi-processor and multi-core architectures; introduction to GPUs)

Course content	
Keywords	
Prerequisites	Mathematical Analysis I, Linear Algebra, Physics I
Propaedeutic courses	
Teaching format	Frontal lectures, exercises, and laboratories
Mandatory attendance	
Specific educational objectives and learning outcomes	The course aims at providing students with the fundamental notions of the organization and architecture of modern computer systems. The students will first acquire basic knowledge about the design and implementation of sequential logical circuits, to then proceed to learn how modern CPUs are organized and2/2 structured. Students will learn how to interface to the CPU at the lowest level possible by means of Assembly programming. Modern and common architectures are introduced, such as x86, ARM, and RISC-V. An architectural understanding of how the CPU interacts with the main memory and peripherals through the system bus is provided
Specific educational objective and learning outcomes (additional information)	Knowledge and understanding The student knows how sequential digital circuits are structured and designed. They know how modern CPU architectures are structured and organized and how to write Assembly programs for at least one common architecture. Applying knowledge and understanding The student is able to use the knowledge acquired to create sequential circuits, to write Assembly programs, and to understand how the tradeoffs in the CPU architecture design affect the performance of their programs. Communication skills The student is able to present the competencies acquired with vocabulary appropriate to the topic. Learning skills The student is able to use the tools and reasoning techniques acquired to extend his/her knowledge.
Assessment	Written exam and lab project. Assessment mode for attending and non-attending student is the same. NOTE: Project work and classroom contributions are valid for 1 academic year and cannot be carried over beyond that time-frame.
Evaluation criteria	The evaluation criteria will be: For the written exam: clarity of understanding, acquired skills, problem solving capabilities. For the lab project: functional correctness of the project w.r.t. the specifications, quality of implementation

Required readings	Materials provided by the teacher.
Supplementary readings	Supplementary readings will be provided by the lecturers prior to lectures.
Further information	
Sustainable Development Goals (SDGs)	